

- 1 What is claimed is:
- 2 1. An amplifier having dual modes of operation, comprising:
- 3 a first differential amplifier receiving a first pair of differential input signals and
- 4 having a first output terminal;
- 5 a second differential amplifier receiving a second pair of differential input signals
- 6 and having a second output terminal; and
- 7 circuitry for coupling the first and second differential amplifiers and controlled by
- 8 a control signal, wherein a first value of the control signal activates the circuitry so that
- 9 the first and second differential amplifiers provide a differential signal at the first and
- 10 second output terminals in response to the first and second pair of differential input
- 11 signals, and wherein a second value of the control signal deactivates the circuitry so that
- 12 the first and second differential amplifiers operate independently to provide single ended
- 13 signals at the first and second output terminals in response to the first and second pair of
- 14 differential input signals, respectively.
- 15 2. The amplifier of claim 1 wherein the first differential amplifier includes:
- 16 a first pair of transistors connected in series; and
- 17 a second pair of transistors connected in series,
- 18 wherein the first pair of transistors is connected in parallel with the second pair of
- 19 transistors.
- 20 3. The amplifier of claim 2 wherein the second differential amplifier includes:
- 21 a third pair of transistors connected in series; and
- 22 a fourth pair of transistors connected in series,
- 23 wherein the third pair of transistors is connected in parallel with the fourth pair of
- 24 transistors.
- 25 4. The amplifier of claim 1 wherein the first differential amplifier includes a first
- 26 transistor and the second differential amplifier includes a second transistor, wherein the
- 27 first and second transistors are connected in parallel, and wherein the control signal
- 28 activates and deactivates the first and second transistors.
- 29 5. The amplifier of claim 1 wherein the circuitry for coupling includes a coupling
- 30 transistor connected to the first and second differential amplifiers, wherein the control
- 31 signal activates and deactivates the coupling transistor.
- 32 6. The amplifier of claim 1, further including:

1 a first coupling circuit, activated and deactivated by the control signal, for
2 providing a short between first corresponding ones of the first and second pairs of
3 differential input signals; and

4 a second coupling circuit, activated and deactivated by the control signal, for
5 providing a short between second corresponding ones of the first and second pairs of
6 differential input signals.

7 7. The amplifier of claim 6 wherein the first and second coupling circuits each
8 include a pair of transistors connected in parallel, wherein the control signal activates and
9 deactivates the pair of transistors.

10 8. The amplifier of claim 1 wherein:
11 the first differential amplifier includes a first pair of transistors connected in series
12 for driving a first signal at the first output terminal; and
13 the second differential amplifier includes a second pair of transistors connected in
14 series for driving a second signal at the second output terminal.

15 9. The amplifier of claim 1 wherein the first and second differential amplifiers each
16 include a circuit element controlled by a power control signal for selectively operating the
17 amplifier in a voltage mode and a current mode.

18 10. The amplifier of claim 1 wherein:
19 the first differential amplifier includes a first pair of transistors for receiving the
20 first pair of differential input signals; and
21 the second differential amplifier includes a second pair of transistors for receiving
22 the second pair of differential input signals.

23 11. The amplifier of claim 1, further including first and second transistors connected
24 in parallel, the first transistor connected with the first differential amplifier and the second
25 transistor connected with the second differential amplifier, wherein the first and second
26 transistors provide current source biasing for the first and second differential amplifiers,
27 respectively.

28 12. An amplifier having dual modes of operation, comprising:
29 a first differential amplifier receiving a first pair of differential input signals and
30 having a first output terminal;
31 a second differential amplifier receiving a second pair of differential input signals
32 and having a second output terminal;
33 a first coupling circuit for coupling first corresponding ones of the first and second
34 pairs of differential input signals; and

1 a second coupling circuit for coupling second corresponding ones of the first and
2 second pairs of differential input signals,

3 wherein the first and second coupling circuits are controlled by a control signal,
4 wherein a first value of the control signal activates the first and second coupling circuits
5 so that the first and second differential amplifiers provide a differential signal at the first
6 and second output terminals in response to the first and second pairs of differential input
7 signals, and wherein a second value of the control signal deactivates the first and second
8 coupling circuits so that the first and second differential amplifiers operate independently
9 to provide single ended signals at the first and second output terminals in response to the
10 first and second pairs of differential input signals, respectively.

11 13. The amplifier of claim 12 wherein the first differential amplifier includes:

12 a first pair of transistors connected in series; and
13 a second pair of transistors connected in series,

14 wherein the first pair of transistors is connected in parallel with the second pair of
15 transistors.

16 14. The amplifier of claim 13 wherein the second differential amplifier includes:

17 a third pair of transistors connected in series; and
18 a fourth pair of transistors connected in series,

19 wherein the third pair of transistors is connected in parallel with the fourth pair of
20 transistors.

21 15. The amplifier of claim 12 wherein the first and second coupling circuits each
22 include a pair of transistors connected in parallel, wherein the control signal activates and
23 deactivates the pair of transistors.

24 16. The amplifier of claim 12 wherein:

25 the first differential amplifier includes a first pair of transistors connected in series
26 for driving a first signal at the first output terminal; and

27 the second differential amplifier includes a second pair of transistors connected in
28 series for driving a second signal at the second output terminal.

29 17. The amplifier of claim 12 wherein the first and second differential amplifiers each
30 include a circuit element controlled by a power control signal for selectively operating the
31 amplifier in a voltage mode and a current mode.

32 18. The amplifier of claim 12 wherein:

33 the first differential amplifier includes a first pair of transistors for receiving the
34 first pair of differential input signals; and

1 the second differential amplifier includes a second pair of transistors for receiving
2 the second pair of differential input signals.

3 19. The amplifier of claim 12, further including first and second transistors connected
4 in parallel, the first transistor connected with the first differential amplifier and the second
5 transistor connected with the second differential amplifier, wherein the first and second
6 transistors provide current source biasing for the first and second differential amplifiers,
7 respectively.

8 20. A method for providing dual modes of operation in an amplifier using only one set
9 of output terminals, comprising:

10 receiving a first pair of differential input signals;
11 receiving a second pair of differential input signals; and
12 using a control signal to provide two modes of operation, the using step including:
13 providing, based upon a first value of the control signal, a differential
14 signal at first and second output terminals in response to the first and second pair
15 of differential input signals; and

16 providing, based upon a second value of the control signal, single ended
17 signals at the first and second output terminals in response to the first and second
18 pair of differential input signals, respectively.